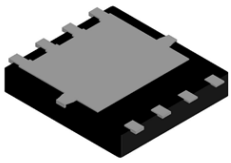
FEATURES

- Drain-Source Withstand Voltage: 40V
- Max. $R_{DS(on)}$: 4.0mΩ @ V_{GS}=10V
  6.0mΩ @ V_{GS}=4.5V
- Trench Technology
- Supper high density cell design
- Low ON resistance
- Low Threshold Voltage
- Package PDFN3333-8L
- 100% UIS and Rg Tested

PRODUCT APPEARANCE



PDFN3333-8L

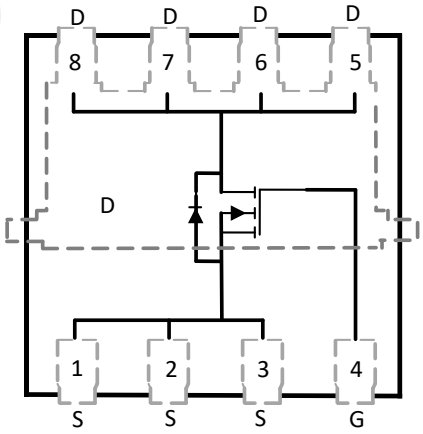
DESCRIPTION

The SNM044R0DRA is N-Channel enhancement MOS Field Effect Transistor. Uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in DC-DC conversion, power switch and charging circuit. Standard Product SNM044R0DRA is in compliance with RoHS.

Applications:

- DC/DC converters
- Power supply converters circuit
- Load/Power Switching for portable device

PIN CONFIGURATION



MARKING

4353 = Device Code
DR = Special Code
Y = Year
M = Month (A~z)

LIMITING VALUES

Parameter	Symbol	Condition	Value	Unit
Drain-Source Voltage	V_{DS}		40	V
Gate-Source Voltage	V_{GS}		±20	V
Continuous Drain Current (4)	I_D	T_C=25°C	95	A
		T_C=100°C	60	A
Pulsed Drain Current (3)	I_{DM}		210	A
Continuous Drain Current	I_D	T_A=25°C	28	A
		T_A=100°C	23	A
Avalanche Energy L=0.3mH	E_{AS}		98.4	mJ
Power Dissipation (2)	P_D	T_C=25°C	63	W
		T_C=100°C	25	W
Power Dissipation (1)	P_D	T_A=25°C	5.5	W
		T_A=100°C	3.5	W
Operating Junction Temperature	T_J		-55 to 150	°C
Storage Temperature Range	T_{STG}		-55 to 150	°C

THERMAL RESISTANCE RATINGS

Single Operation					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Junction-to-Ambient Thermal Resistance (1)	t ≤10s		17.6	22.9	°C/W
	Steady State	$R_{\theta JA}$	43.3	54.1	
Junction-to-Case Thermal Resistance	Steady State	$R_{\theta JC}$	1.6	2.0	

ELECTRONICS CHARACTERISTICS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 250μA	40			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40V, V_{GS} = 0V			1	μA
Gate-to-source Leakage Current	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS}=V_{DS}, I_D= 250μA	1.3	1.7	2.1	V
Drain-to-source On-resistance (5)	$R_{DS(on)}$	V_{GS} =10V, I_D =20A		3.2	4.0	mΩ
		V_{GS} =4.5V, I_D =20A		4.6	6.0	
CHARGES, CAPACITANCES AND GATE RESISTANCE (6)						
Input Capacitance	C_{ISS}	V_{GS} = 0V, f = 1.0MHz, V_{DS}=25 V		1860		pF
Output Capacitance	C_{OSS}			418		
Reverse Transfer Capacitance	C_{RSS}			13.4		
Total Gate Charge	$Q_{G(10V)}$	V_{GS}=10V, V_{DS}= 20V, I_D =20A		24.6		nC
Total Gate Charge	$Q_{G(4.5V)}$			11.7		
Gate-to-Source Charge	Q_{GS}			5.1		
Gate-to-Drain Charge	Q_{GD}			2.7		
Gate Resistance	Rg	f = 1MHz		1.55		Ω
SWITCHING CHARACTERISTICS (6)						

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Turn-On Delay Time	td(ON)	V_{GS} = 20V, V_{DS} = 10V, I_D = 20A, R_{GEN} = 1.6Ω		5.6		ns
Rise Time	tr			46.6		
Turn-Off Delay Time	td(OFF)			25.6		
Fall Time	tf			13.0		
BODY DIODE CHARACTERISTICS						
Forward Voltage	V_{SD}	V_{GS}=0V, I_S=20A	0.5	0.8	1.2	V
Maximum Continuous Currents	I_S				62	A
Body Diode Reverse Recovery Time (6)	trr	I_F=20A, di/dt= 100A/μs		23.7		ns
Body Diode Reverse Recovery Charge (6)	Qrr	I_F=20A, di/dt= 100A/μs		12.3		nC

(T_J=25℃, unless otherwise noted.)

Note:

(1) FR-4 board (38mm×38mm×t1.6mm, 70μm Copper) partially covered with copper (645mm^2 area).

(2) The power dissipation P_D is based on $T_{J(MAX)}$=150℃, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

(3) Repetitive rating, ~10us pulse width, duty cycle ~1%, keep initial T_J=25℃, the maximum allowed junction temperature of 150℃.

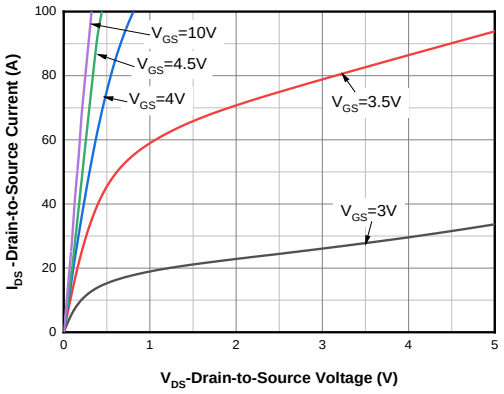
(4) The power dissipation P_{DSM} is based on Junction-to-Ambient thermal resistance $R_{\theta JA}$ t≤10s value and the $T_{J(MAX)}$=150℃.

(5) The static characteristics are obtained using ~380μs pulse, duty cycle ~1%.

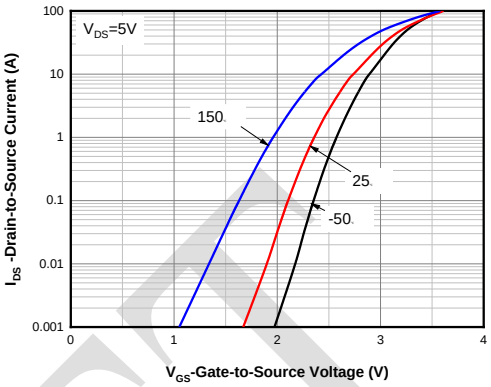
(6) The parameter is not subject to production test – verified by design / characterization.

TYPICAL CHARACTERISTICS

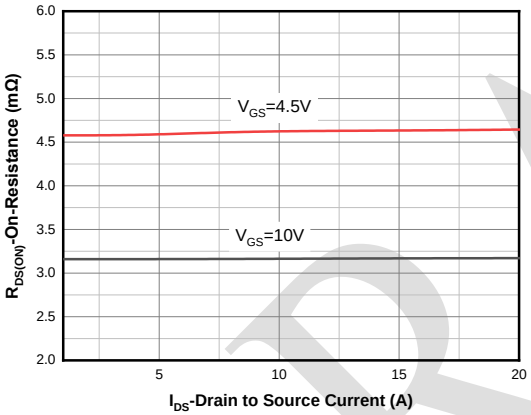
Ta=25℃, unless otherwise noted.



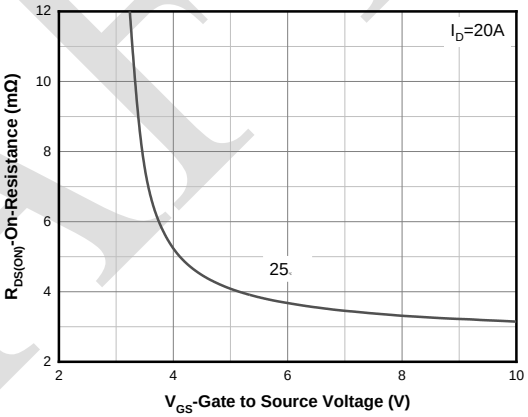
Output Characteristics (5)



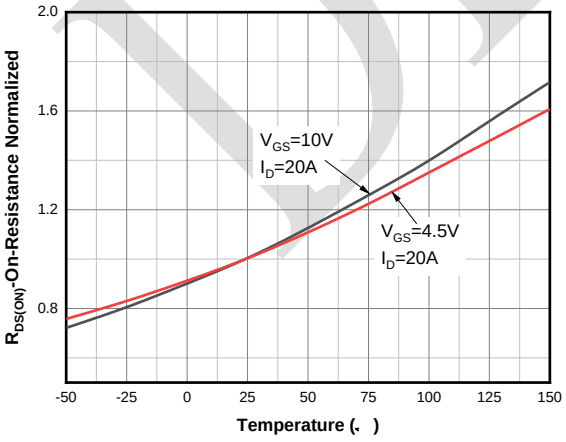
Transfer Characteristics (5)



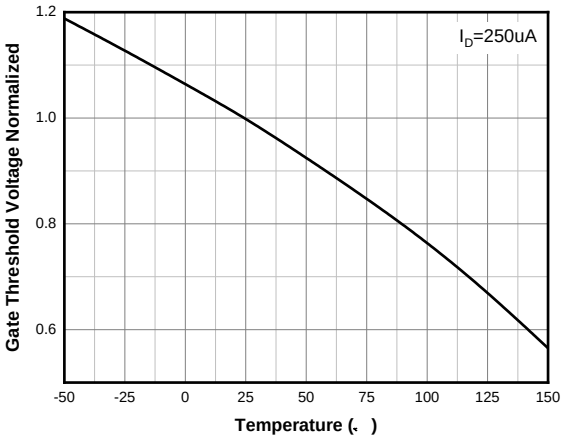
On-Resistance vs. Drain Current (5)



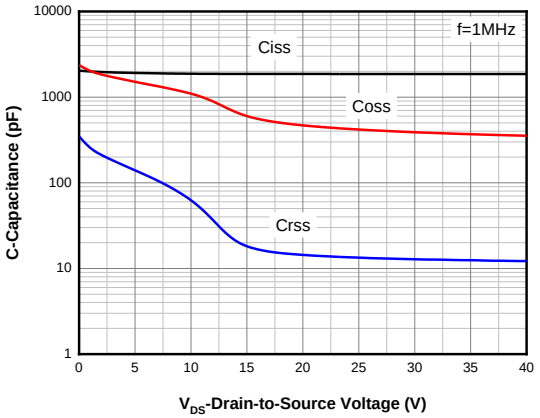
On-Resistance vs. Gate-to-Source Voltage (5)



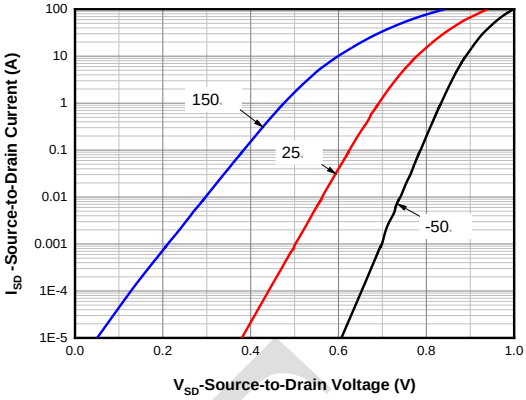
On-Resistance vs. Junction Temperature (5)



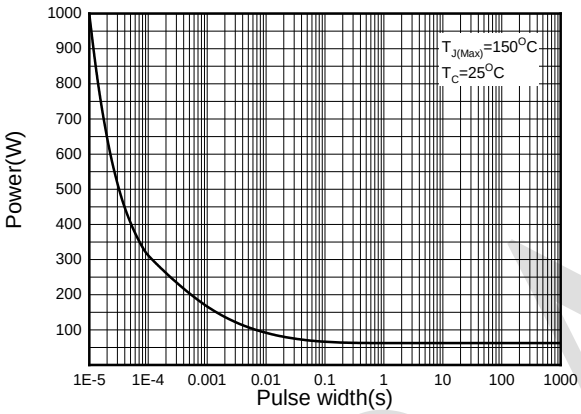
Threshold Voltage vs. Temperature



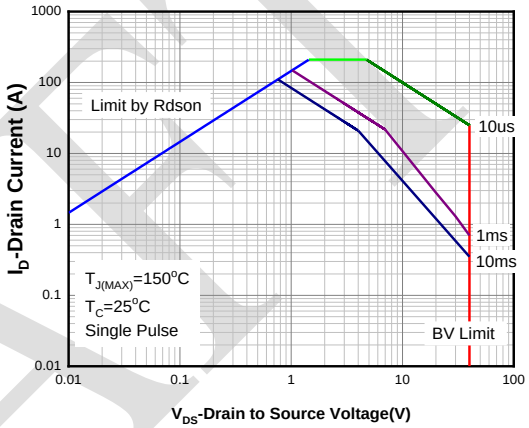
Capacitance



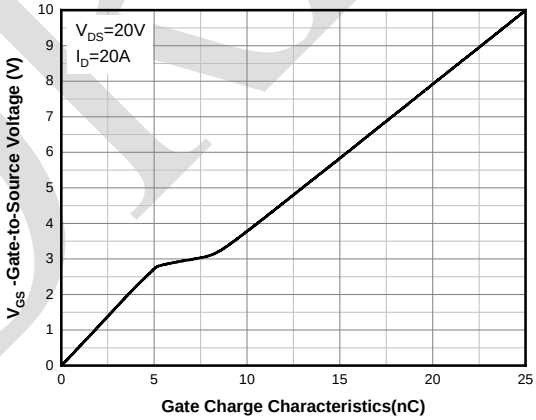
Body Diode Forward Voltage (5)



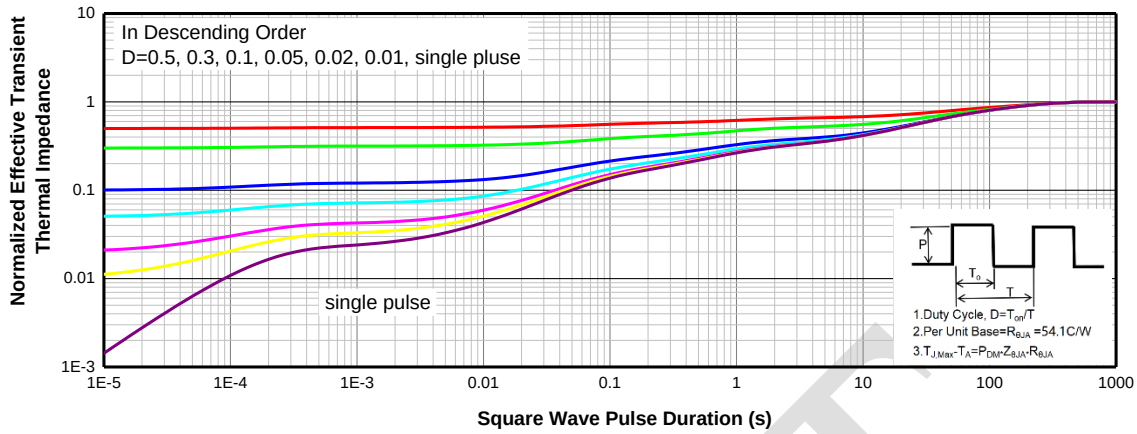
Single Pulse power



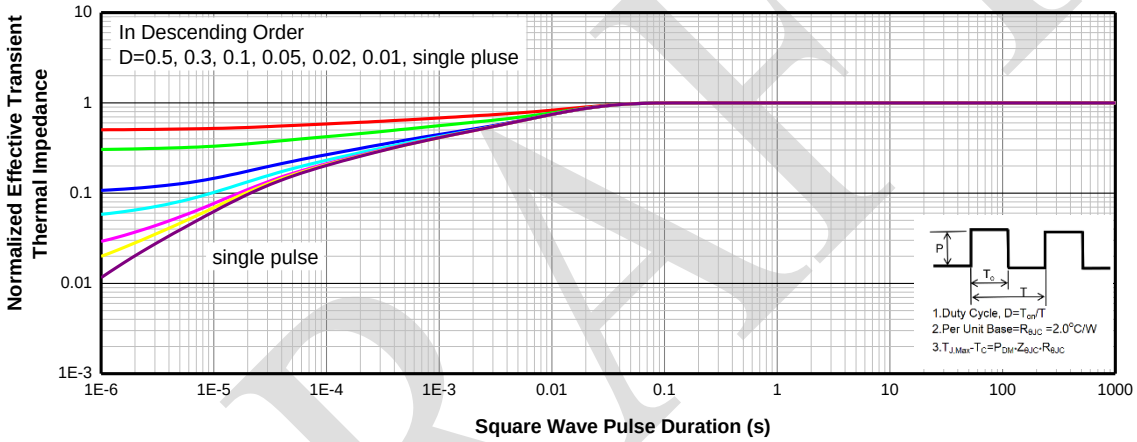
Safe Operating Area



Gate Charge Characteristics



Transient Thermal Response (Junction-to-Case)

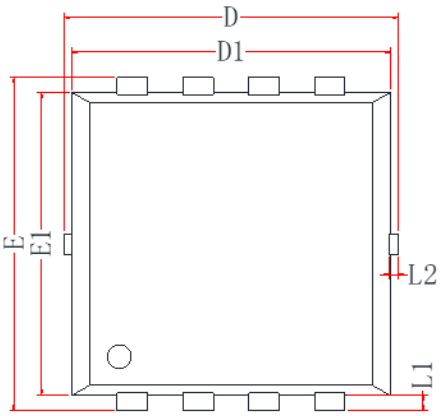


Transient Thermal Response (Junction-to-Ambient)

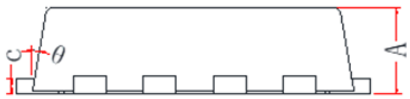
PDFN3333-8L DIMENSIONS

PACKAGE SIZE

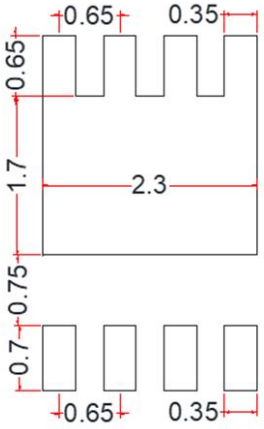
Symbol	Min.	Typ.	Max.
A	0.70	0.80	0.90
b	0.25	0.30	0.39
c	0.14	0.15	0.20
D	3.10	3.30	3.50
D1	3.05	3.15	3.25
D2	2.15	2.25	2.35
e	0.55	0.65	0.75
E	3.10	3.30	3.50
E1	2.90	3.00	3.10
E2	1.60	1.70	1.80
H	0.25	0.40	0.55
K	0.65	0.75	0.85
L	0.30	0.45	0.60
L1	0.05	0.15	0.25
L2	-	-	0.15
θ	8°	10°	12°



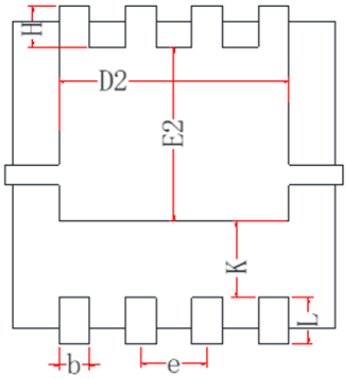
TOP VIEW



SIDE VIEW



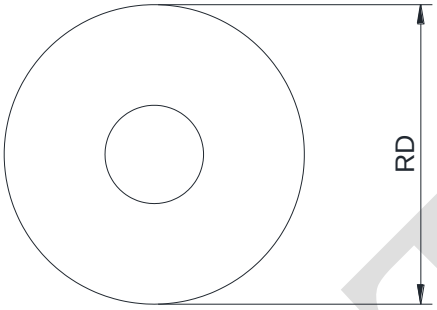
RECOMMENDED LAND PATTERN(Unit:mm)



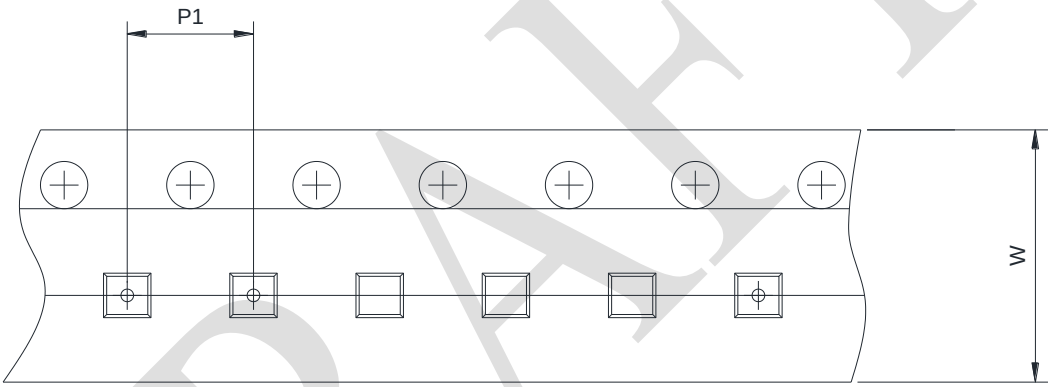
BOTTOM VIEW

TAPE AND REEL INFORMATION

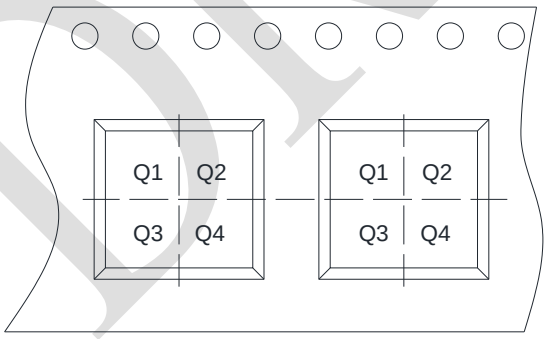
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



User Direction of Feed

RD	Reel Dimension	☐ 7inch ☑ 13inch
W	Overall width of the carrier tape	☐ 8mm ☑ 12mm ☐ 16mm
P1	Pitch between successive cavity centers	☐ 2mm ☐ 4mm ☑ 8mm
Pin1	Pin1 Quadrant	☑ Q1 ☐ Q2 ☐ Q3 ☐ Q4

ORDERING INFORMATION

TYPE NUMBER	PACKAGE	PACKING
SNM044R0DRA-8/TR	PDFN3333-8L	Tape and reel

PDFN3333-8L is packed with 5000 pieces/disc in braided packaging.

Important statement

SIT reserves the right to change the above-mentioned information without prior notice.

REVISION HISTORY

Version number	Datasheet status	Revision date
V0.1	Draft version.	June 2024